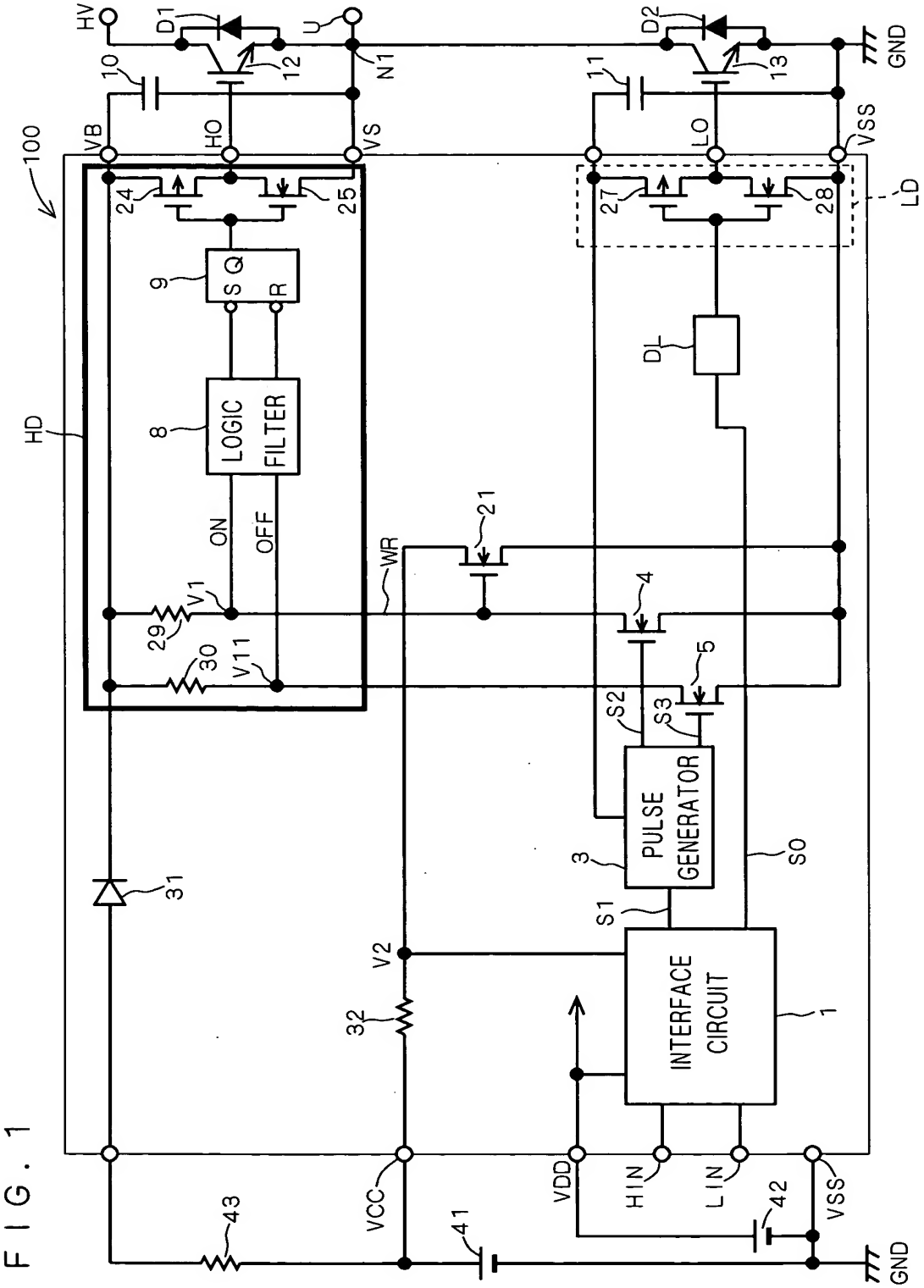

HV
D1
U
D2
GND
10
12
N1
11
13
VB
HO
VS
LO
VSS
100
24
25
27
28
LD
9
S Q
R
DL
8
LOGIC
FILTER
HD
ON
OFF
21
WR
V1
29
30
V11
4
5
S2
S3
PULSE
GENERATOR
3
S0
S1
31
V2
32
INTERFACE
CIRCUIT
1
VDD
HIN
LIN
VSS
42
43
VCC
41
GND

FIG. 1

FIG. 2

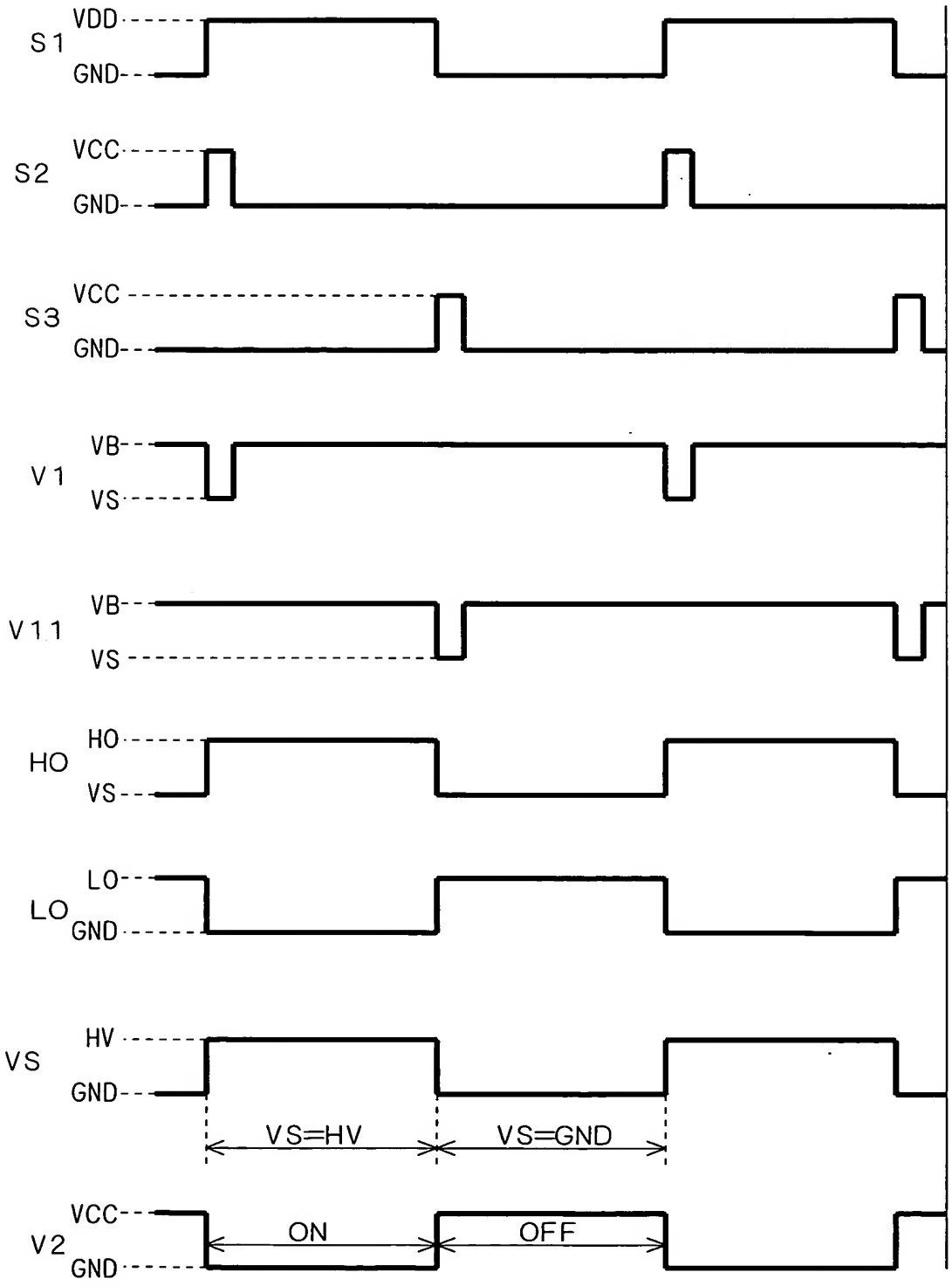

S1
VDD
GND
S2
VCC
GND
S3
VCC
GND
V1
VB
VS
V11
VB
VS
HO
HO
VS
LO
LO
GND
VS
HV
GND
VS=HV
VS=GND
V2
VCC
GND
ON
OFF

FIG. 3

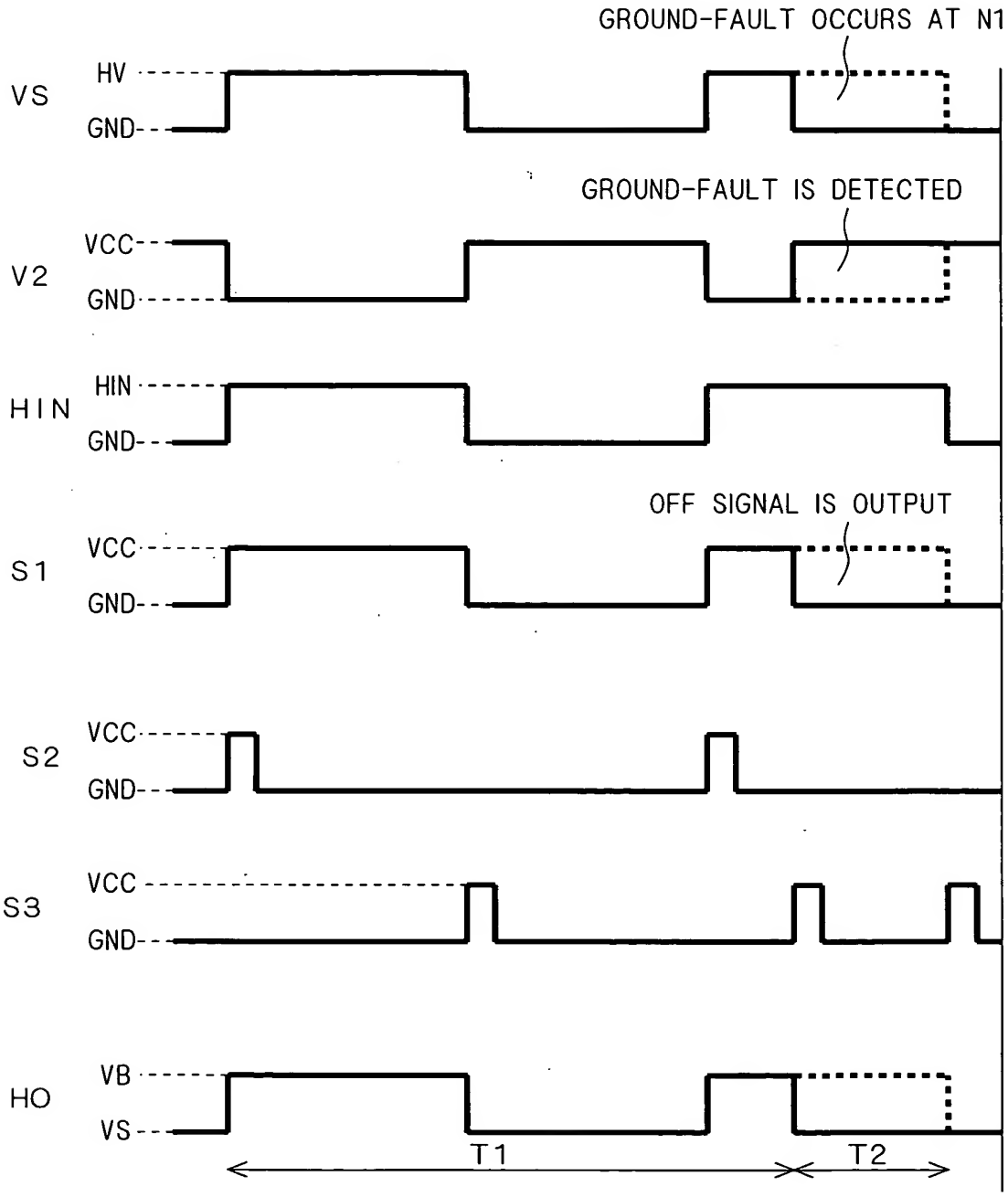
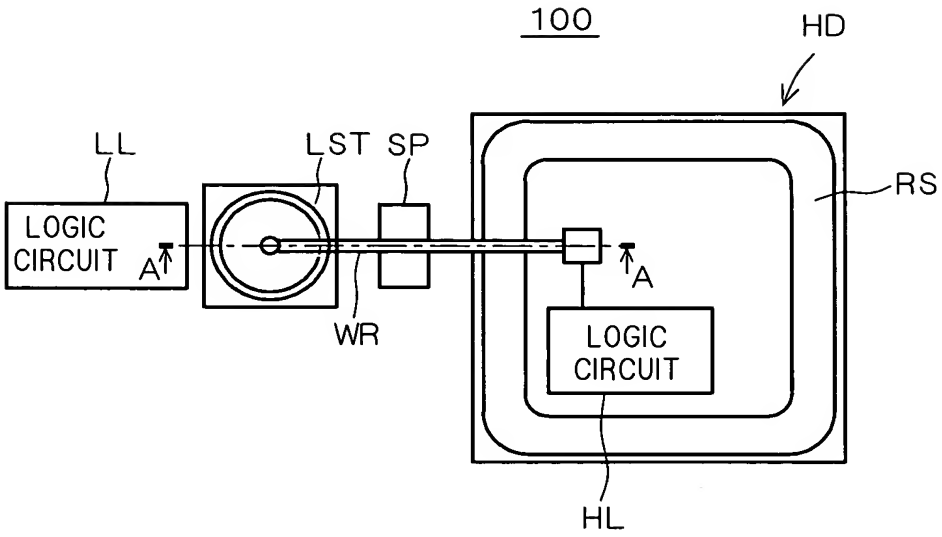

GROUND-FAULT OCCURS AT N1
VS
HV
GND
GROUND-FAULT IS DETECTED
V2
VCC
GND
HIN
HIN
GND
OFF SIGNAL IS OUTPUT
S1
VCC
GND
S2
VCC
GND
S3
VCC
GND
HO
VB
VS
T1
T2

FIG. 4



100

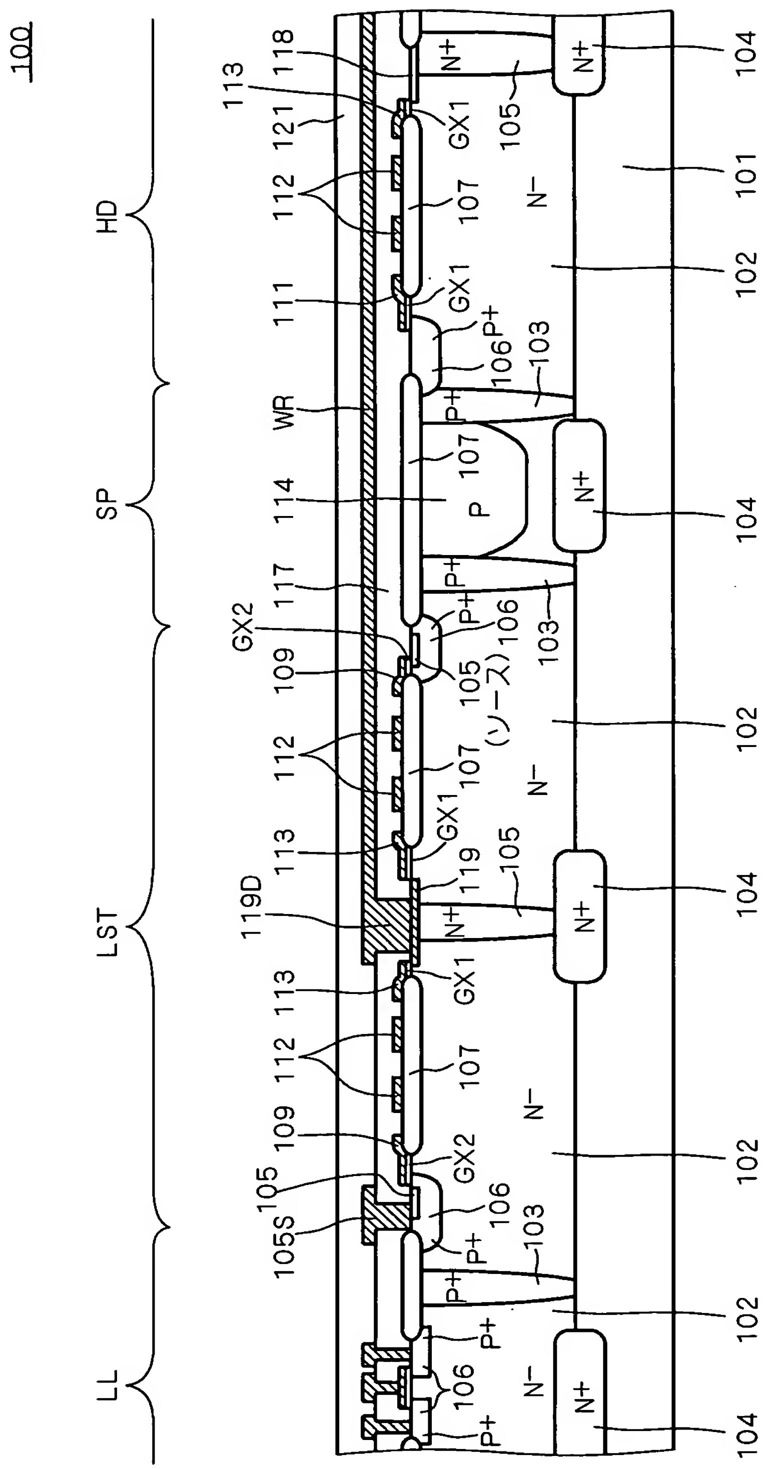

LL
LST
SP
HD
118
113
121
112
111
WR
114
117
GX2
109
119D
105S
105
106
P+
N+
N−
P
GX1
107
103
104
101
102
119
(ソース)

FIG. 5

FIG. 6

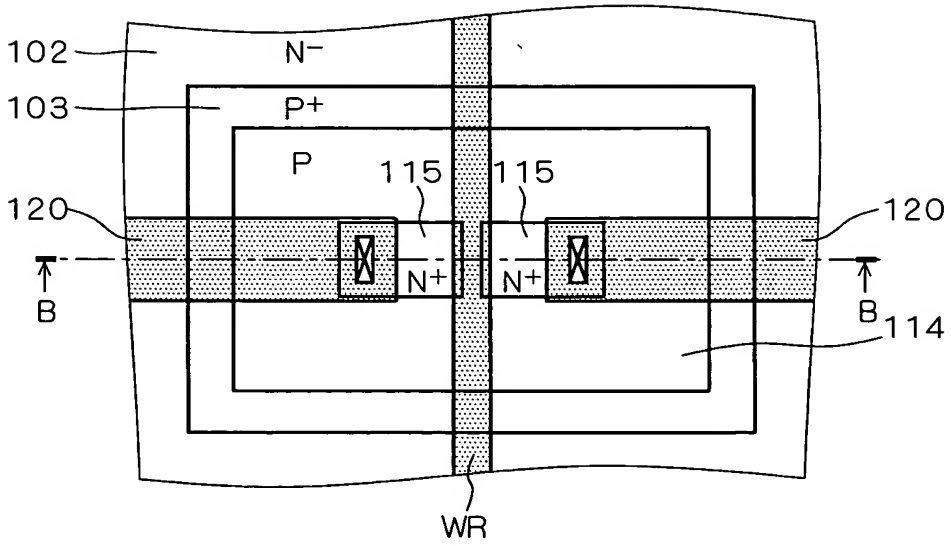
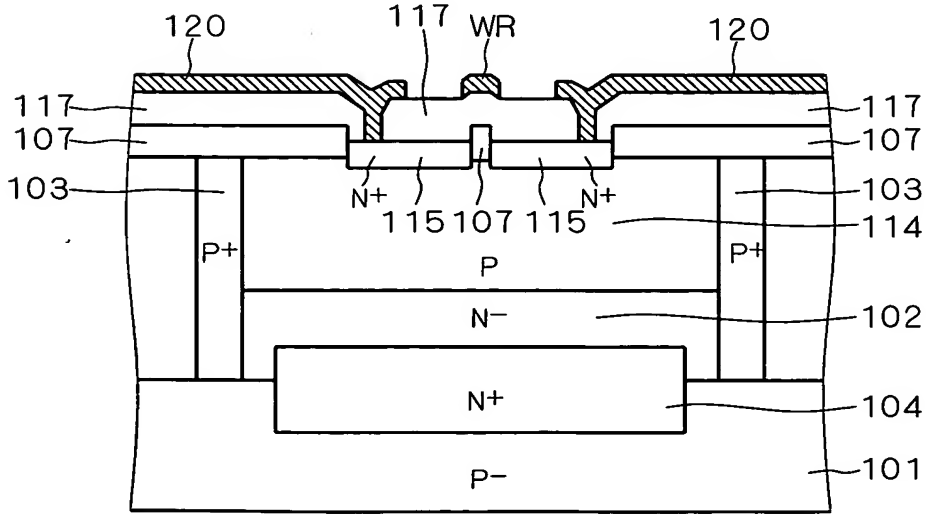

102
N−
103
P+
P
115
115
120
120
B
B
N+
N+
114
WR

FIG. 7


120
117
WR
120
117
117
107
107
103
103
N+
N+
115
107
115
114
P+
P+
P
N−
102
N+
104
P−
101

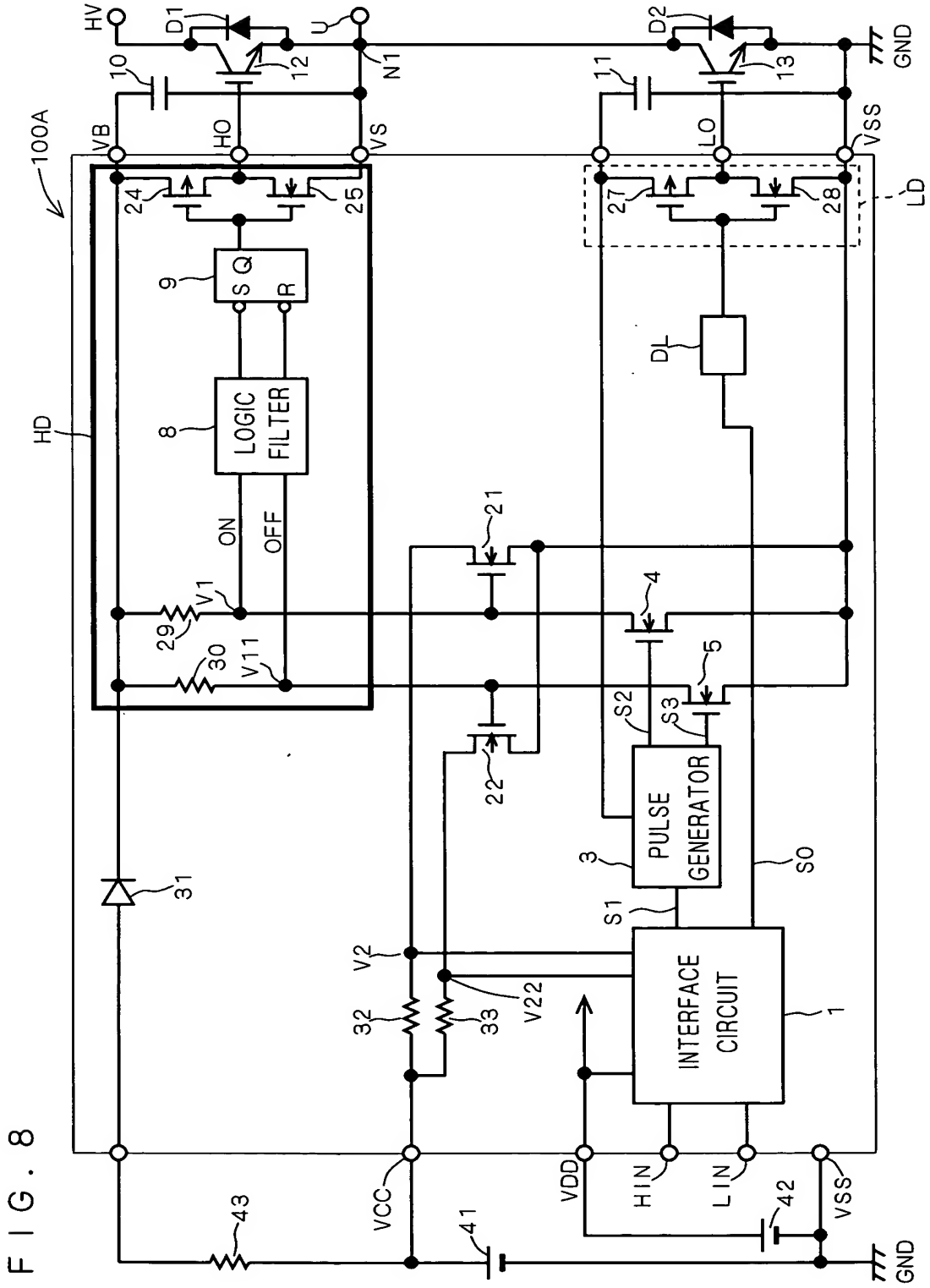

HV
D1
U
D2
GND
10
12
N1
11
13
100A
VB
HO
VS
LO
VSS
LD
24
25
27
28
9
S Q
R
DL
HD
8
LOGIC
FILTER
ON
OFF
21
V1
29
4
30
V11
5
S2
S3
22
PULSE
GENERATOR
3
S0
31
S1
V2
INTERFACE
CIRCUIT
1
32
33
V22
VDD
HIN
LIN
VSS
42
VCC
41
43
GND

FIG. 8

FIG. 9

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

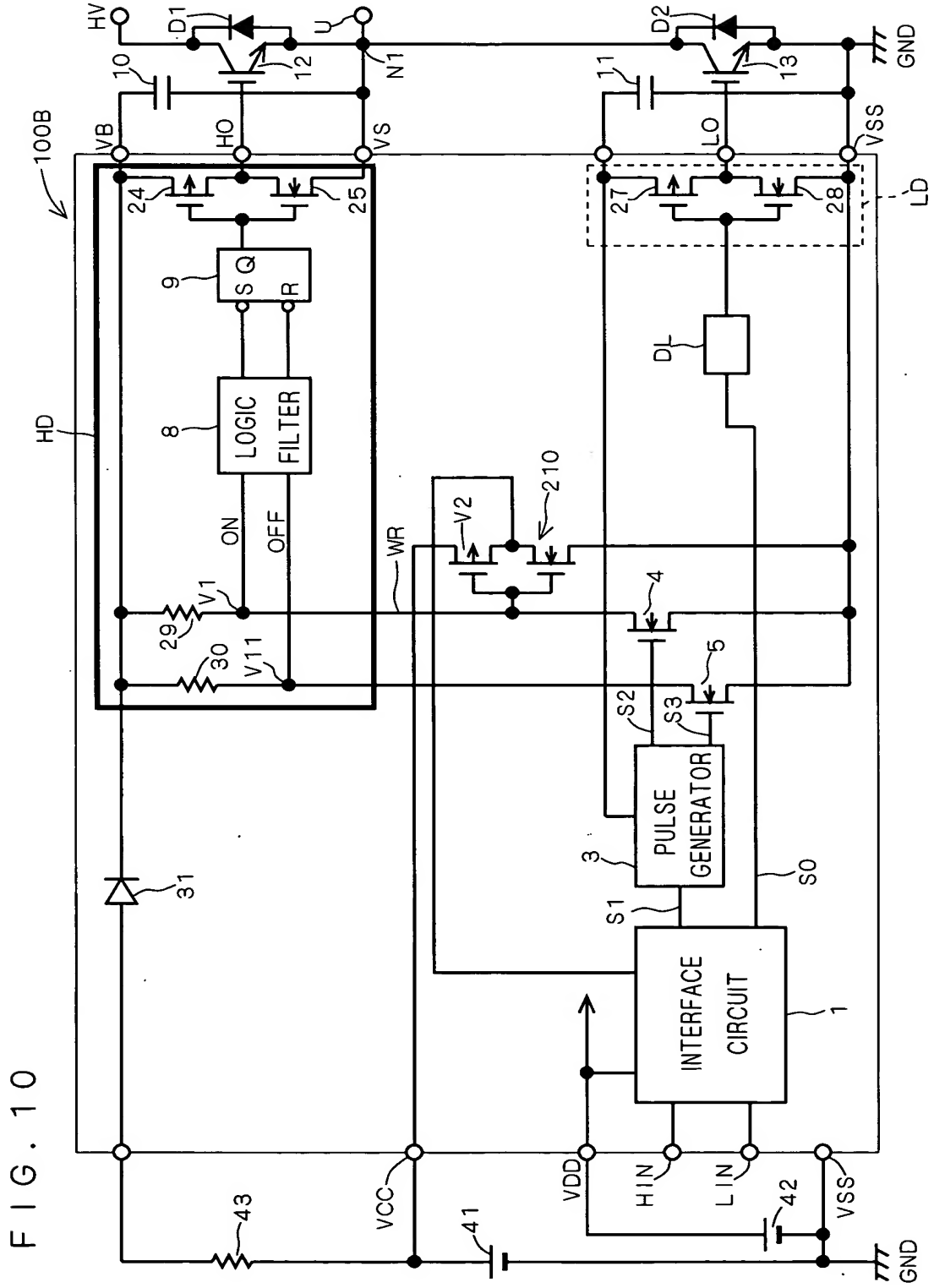

HV
D1
U
D2
GND
10
12
N1
11
13
100B
VB
HO
VS
LO
VSS
LD
24
25
27
28
9
S Q
R
DL
8
LOGIC
FILTER
HD
210
V2
ON
OFF
WR
V1
29
30
V11
4
5
S2
S3
PULSE
GENERATOR
3
S0
S1
31
INTERFACE
CIRCUIT
1
VDD
HIN
LIN
VSS
42
43
VCC
41
GND

FIG. 10

FIG. 11

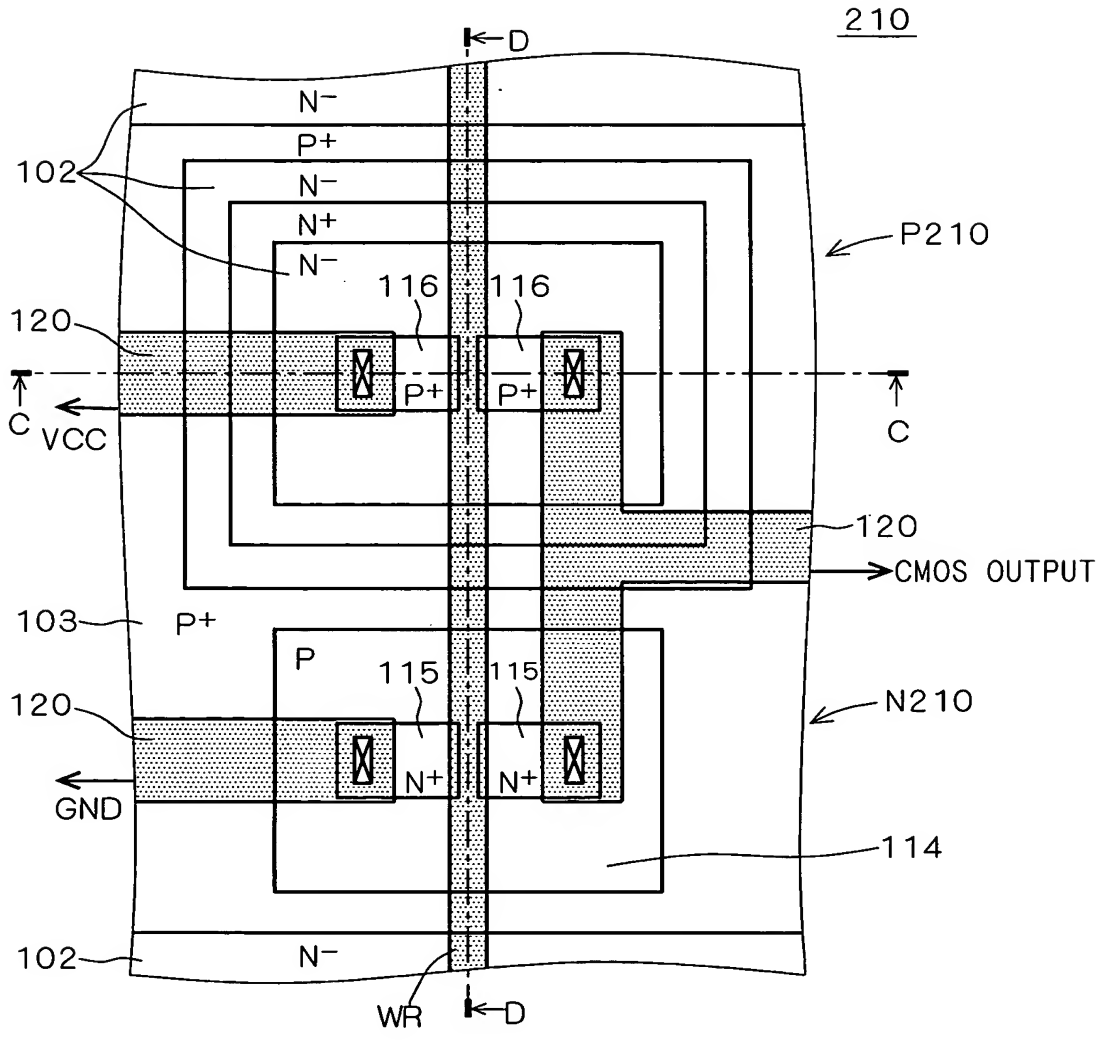

210
D
N−
P+
N−
N+
N−
102
P210
116
116
120
P+
P+
C
VCC
C
120
CMOS OUTPUT
103
P+
P
115
115
120
N210
N+
N+
GND
114
102
N−
WR
D

FIG. 12

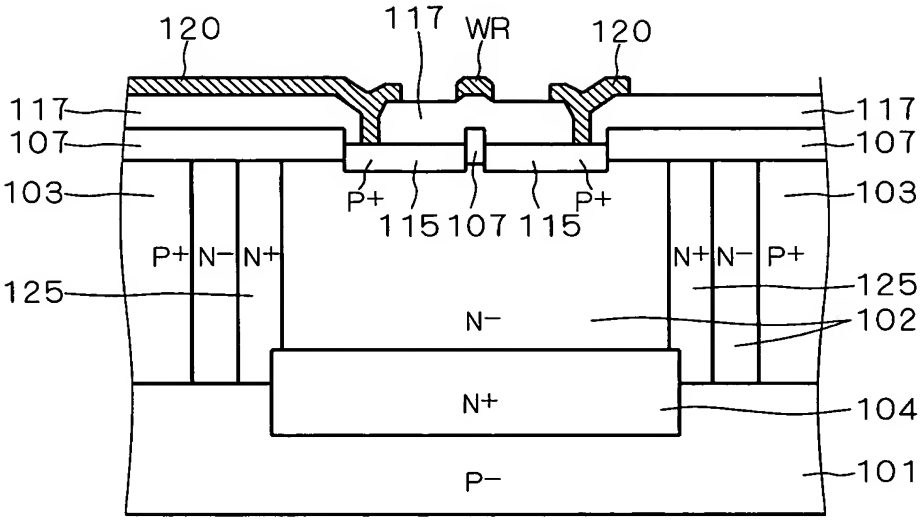
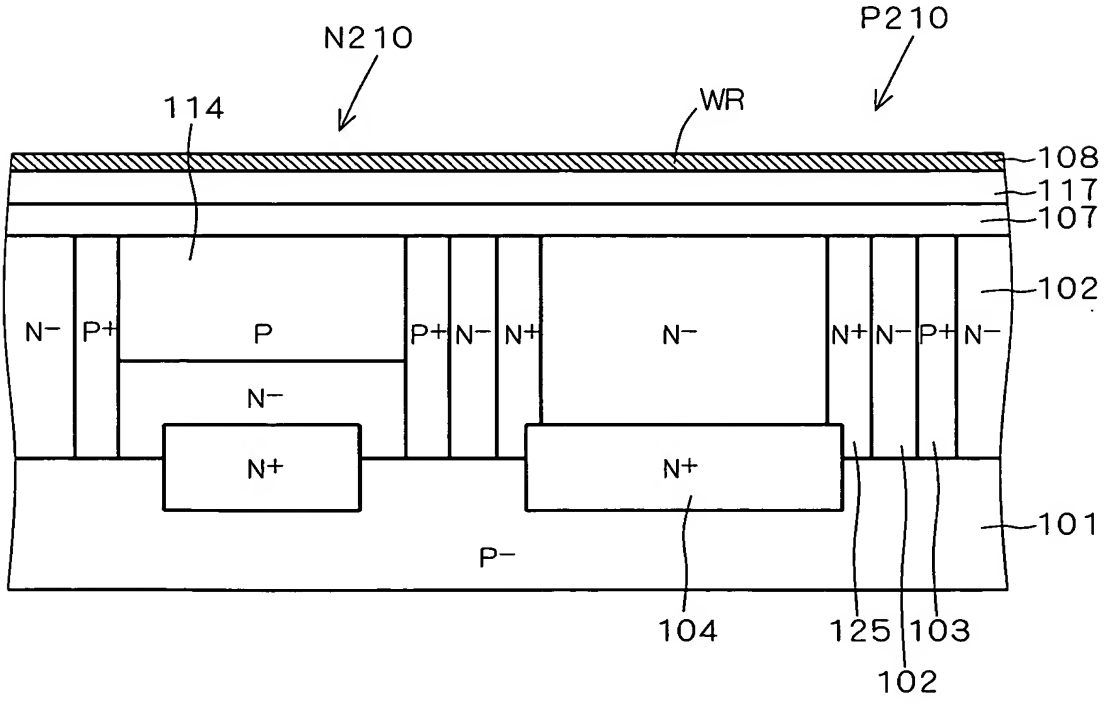

120
117
WR
120
117
117
107
107
103
103
P+
115
107
115
P+
P+
N−
N+
N+
N−
P+
125
125
N−
102
N+
104
P−
101

FIG. 13


N210
P210
114
WR
108
117
107
102
N−
P+
P
P+
N−
N+
N−
N+
N−
P+
N−
N−
N+
N+
101
P−
104
125
103
102

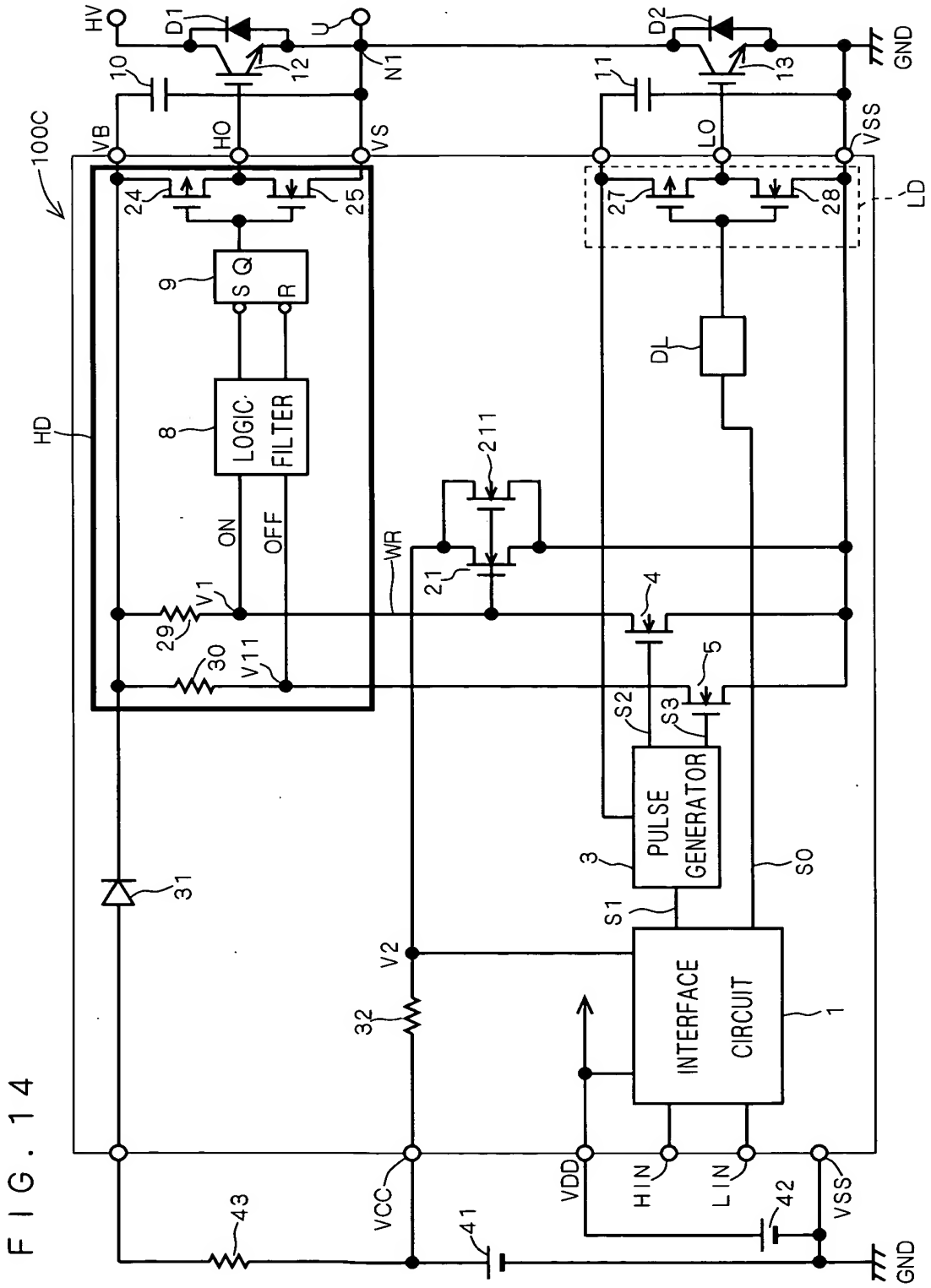

HV
D1
U
D2
GND
10
12
N1
11
13
100C
VB
HO
VS
LO
VSS
LD
24
25
27
28
9
S Q
R
DL
HD
8
LOGIC
FILTER
211
ON
OFF
WR
21
4
V1
29
30
V11
5
S2
S3
PULSE
GENERATOR
3
S0
31
S1
V2
32
INTERFACE
CIRCUIT
1
VDD
HIN
LIN
42
VSS
43
VCC
41
GND

FIG. 14

FIG. 15

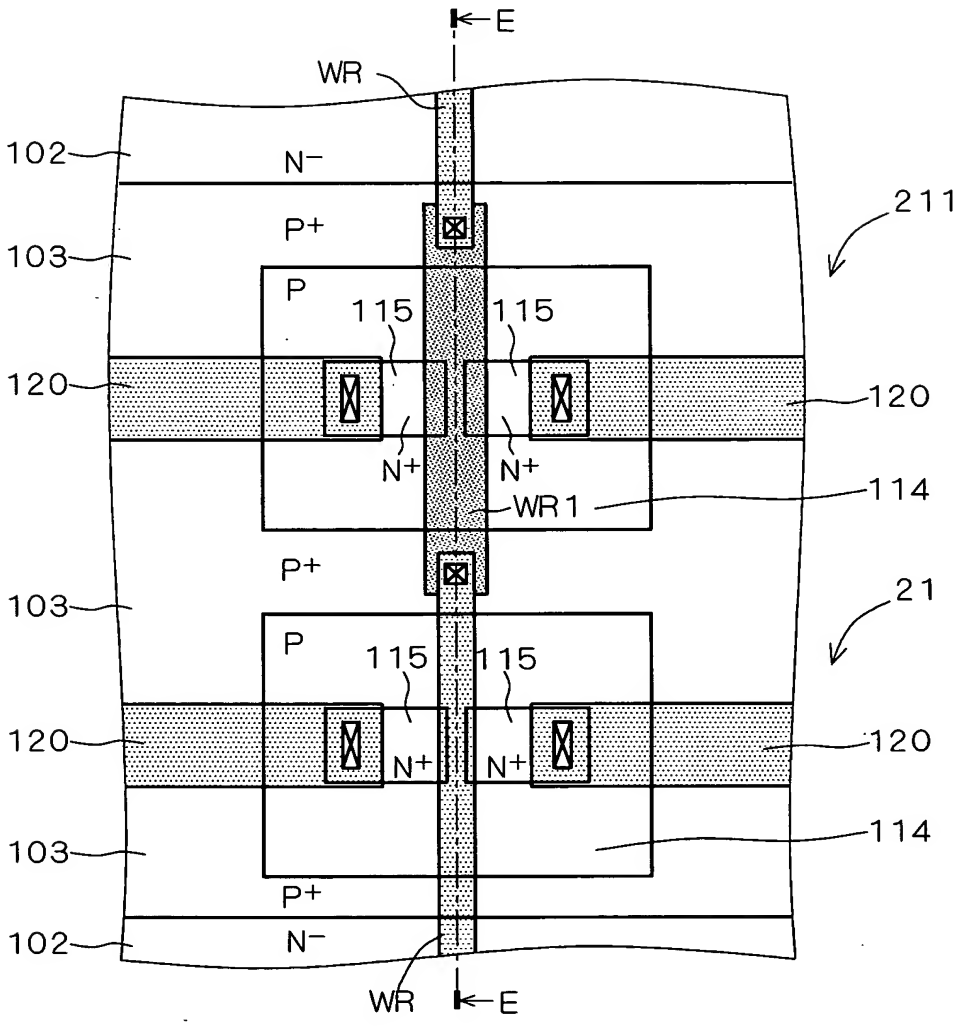

E
WR
102
N−
211
P+
103
P
115
115
120
120
N+
N+
WR1
114
P+
103
21
P
115
115
120
120
N+
N+
103
114
P+
102
N−
WR
E

FIG. 16

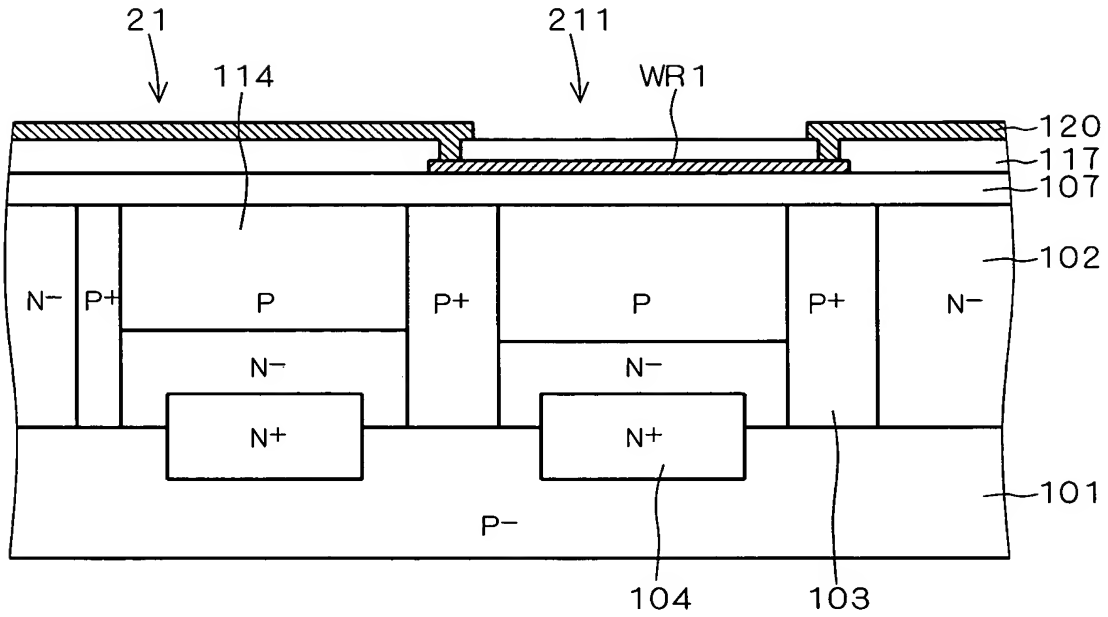


FIG. 17

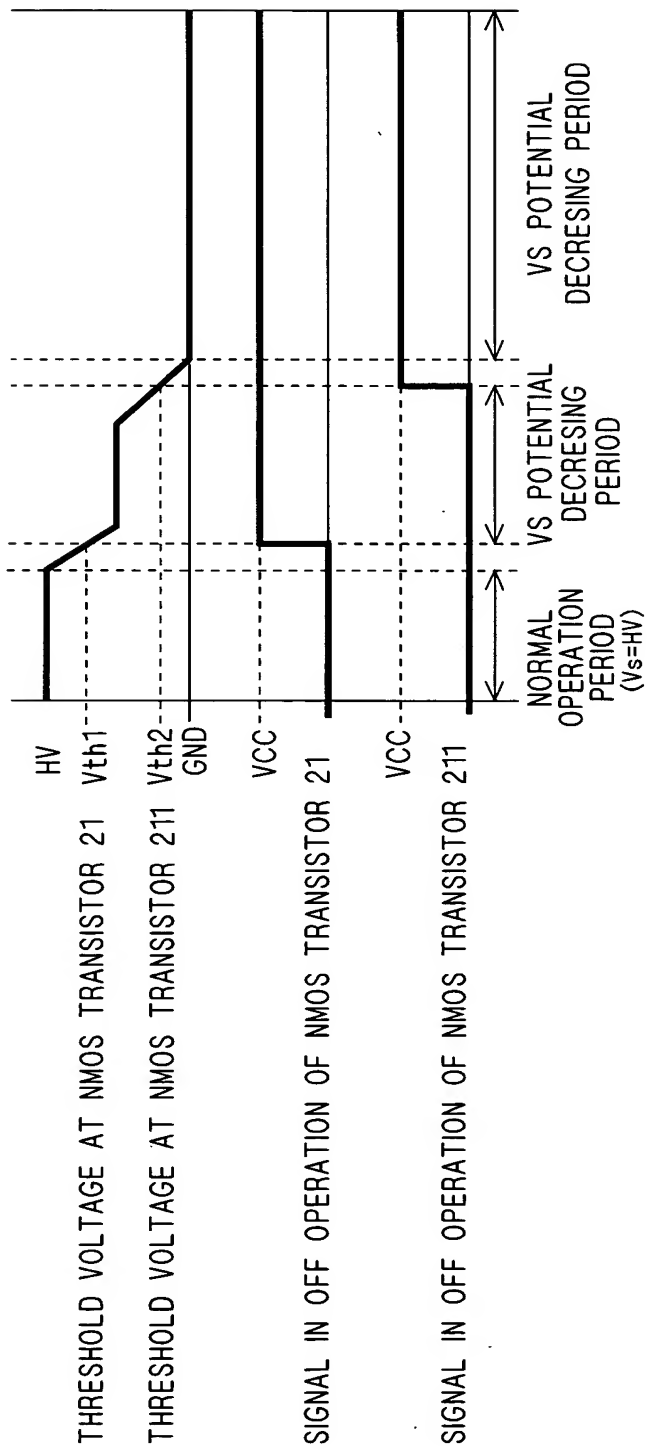

HV
Vth1
Vth2
GND
VCC
VCC
THRESHOLD VOLTAGE AT NMOS TRANSISTOR 21
THRESHOLD VOLTAGE AT NMOS TRANSISTOR 211
SIGNAL IN OFF OPERATION OF NMOS TRANSISTOR 21
SIGNAL IN OFF OPERATION OF NMOS TRANSISTOR 211
NORMAL OPERATION PERIOD (Vs=HV)
VS POTENTIAL DECRESING PERIOD
VS POTENTIAL DECRESING PERIOD

FIG. 18

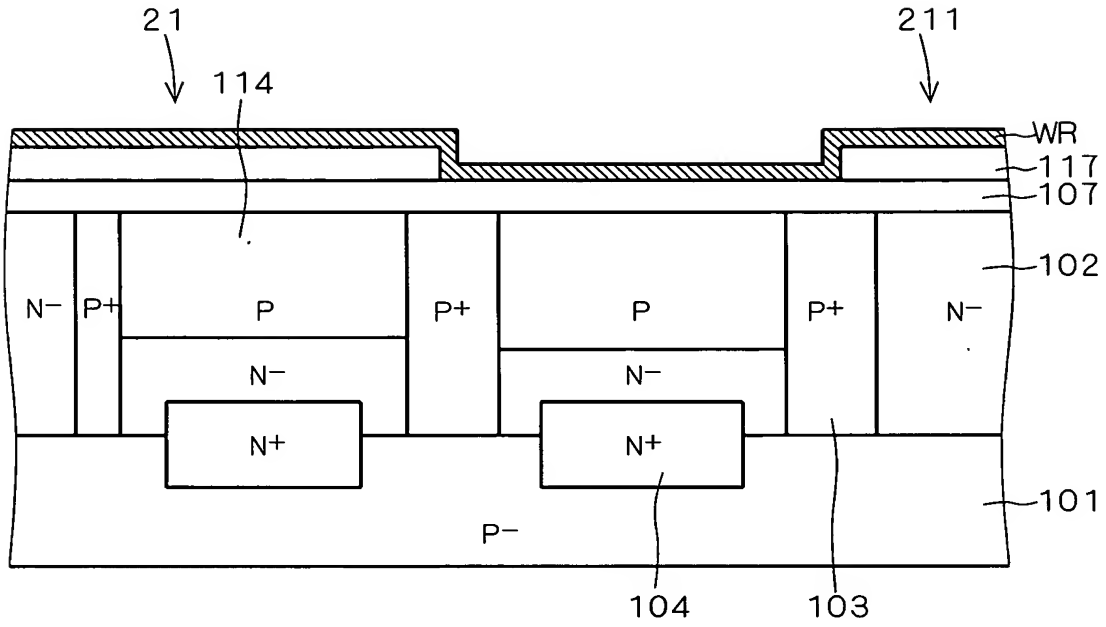

21
114
211
WR
117
107
102
N−
P+
P
P+
P
P+
N−
N−
N−
N+
N+
101
P−
104
103

FIG. 19

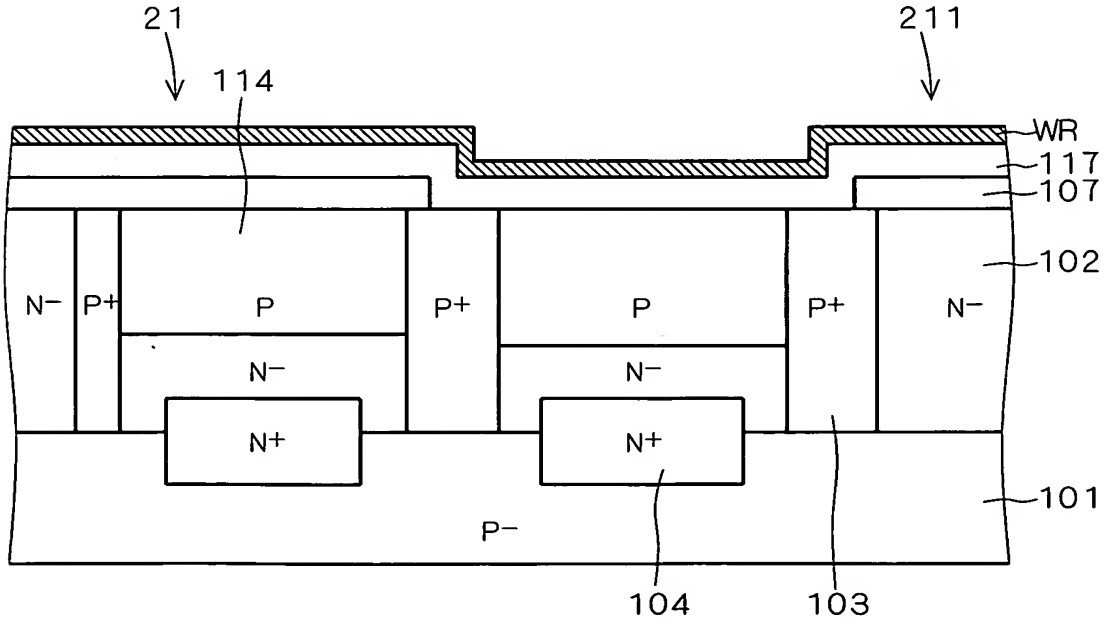

21
114
211
WR
117
107
102
N−
P+
P
P+
P
P+
N−
N−
N−
N+
N+
101
P−
104
103

FIG. 20

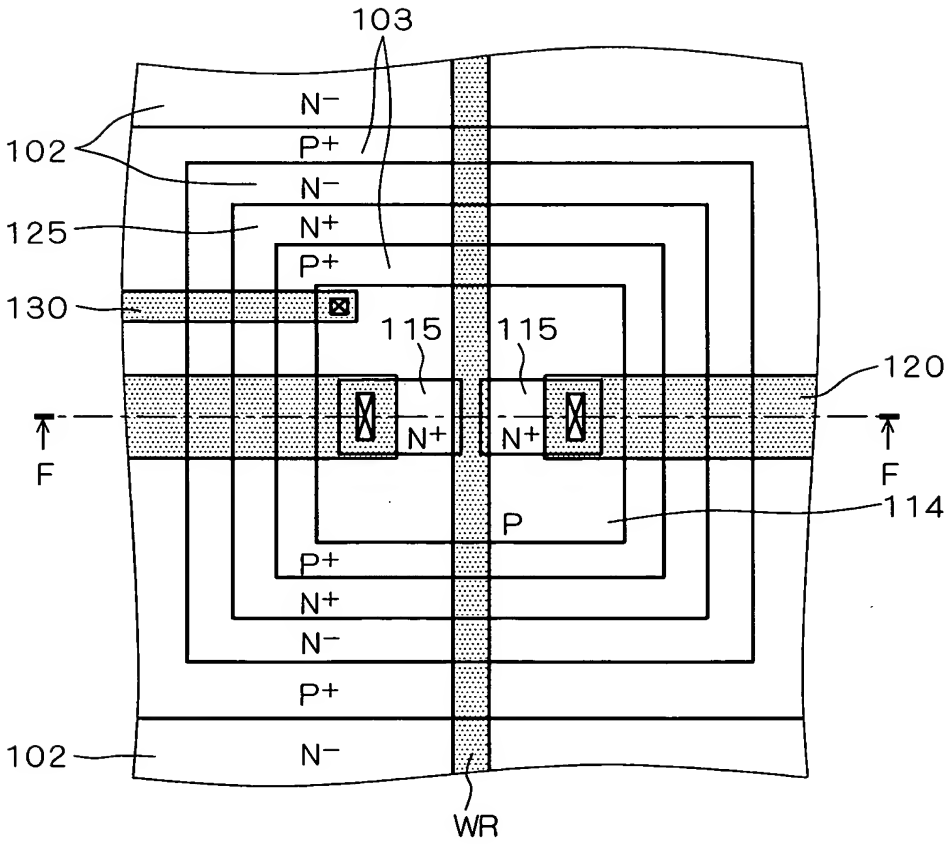


FIG. 21

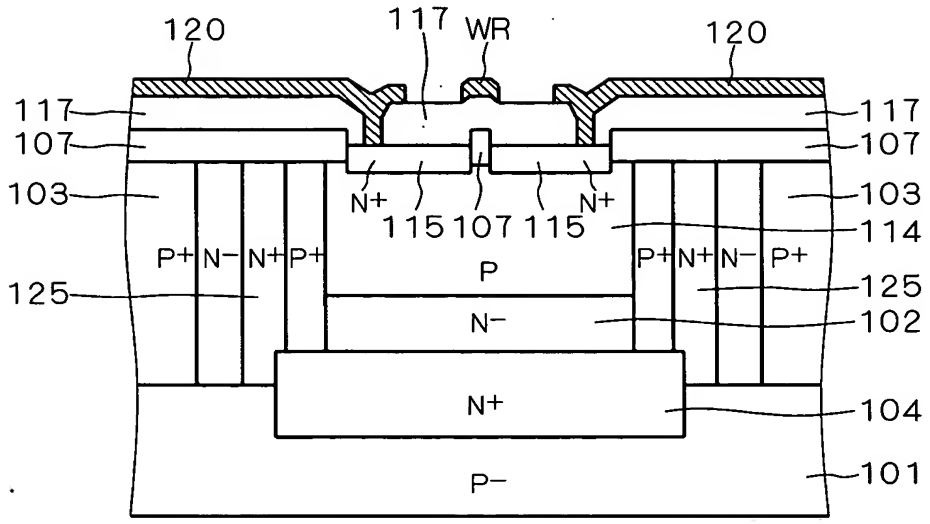
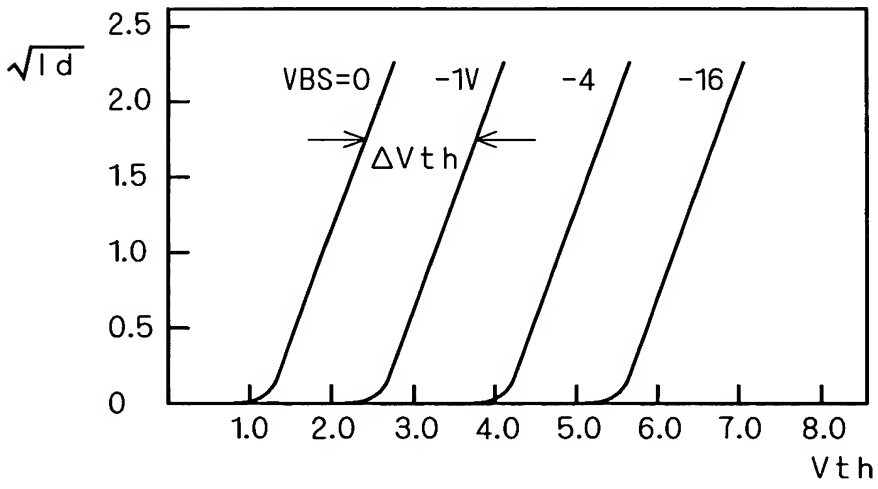

120
117
WR
120
117
107
103
N+
115
107
115
N+
117
107
103
114
P+
N−
N+
P+
P
P+
N+
N−
P+
125
125
N−
102
N+
104
P−
101

FIG. 22


√Id
2.5
2.0
1.5
1.0
0.5
0
VBS=0
-1V
-4
-16
ΔVth
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
Vth

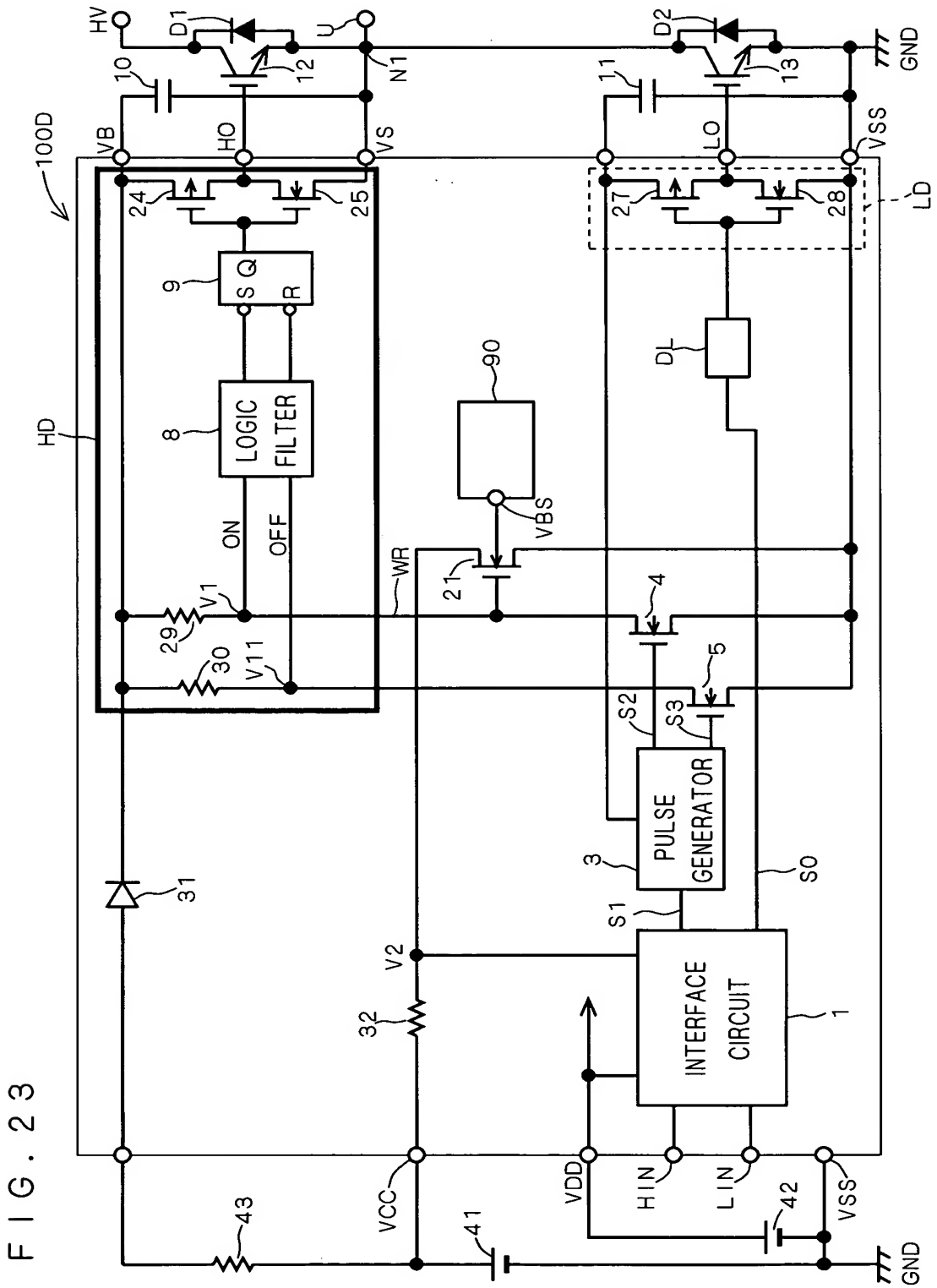
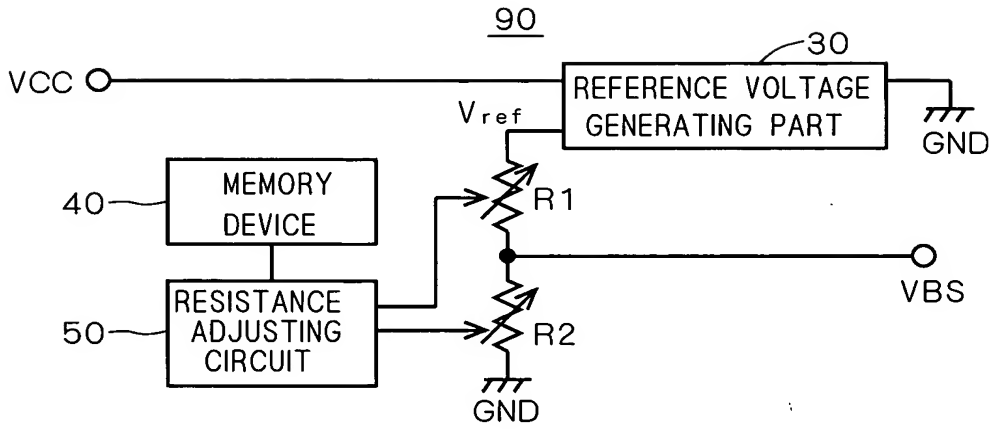

HV
D1
U
N1
D2
GND
10
12
11
13
100D
VB
HO
VS
LO
VSS
LD
24
25
27
28
9
S
Q
R
DL
90
8
LOGIC
FILTER
HD
ON
OFF
VBS
WR
21
4
V1
29
30
V11
5
S2
S3
PULSE
GENERATOR
3
S0
S1
31
V2
32
INTERFACE
CIRCUIT
1
VDD
HIN
LIN
VSS
42
43
VCC
41
GND

FIG. 23

FIG. 24


90
30
VCC
REFERENCE VOLTAGE GENERATING PART
GND
Vref
40
MEMORY DEVICE
R1
VBS
50
RESISTANCE ADJUSTING CIRCUIT
R2
GND

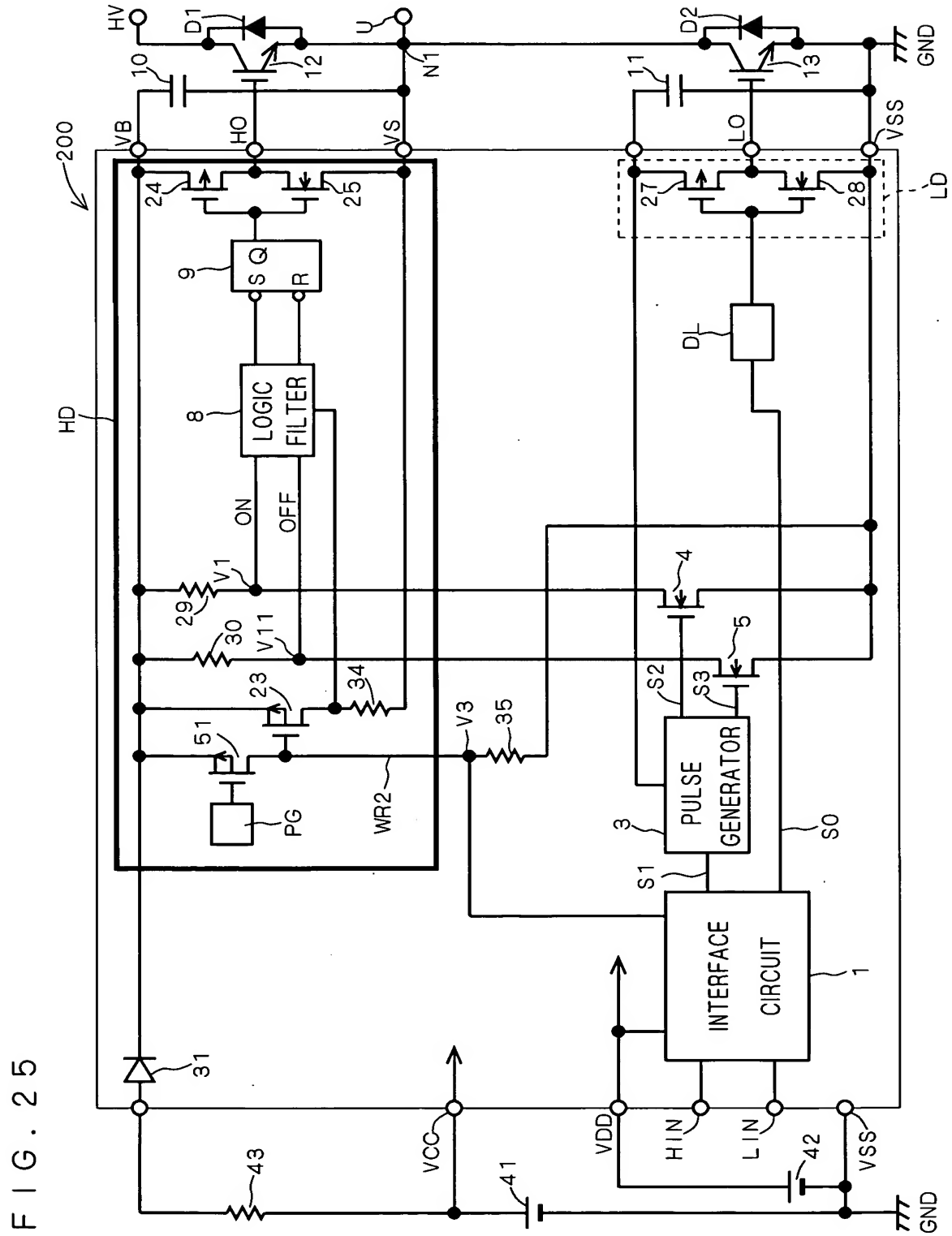

HV
D1
U
D2
GND
10
12
N1
11
13
200
VB
HO
VS
LO
VSS
LD
24
25
27
28
9
S Q
R
DL
HD
8
LOGIC
FILTER
ON
OFF
V1
29
30
V11
4
5
S2
S3
23
34
V3
35
51
PG
WR2
PULSE
GENERATOR
3
S0
S1
INTERFACE
CIRCUIT
1
31
VCC
VDD
HIN
LIN
42
VSS
43
41
GND

FIG. 25

FIG. 26

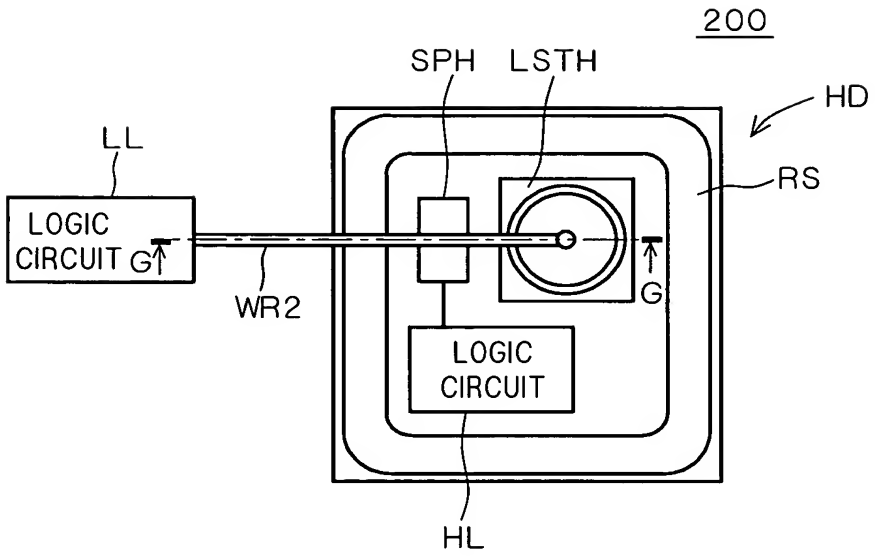
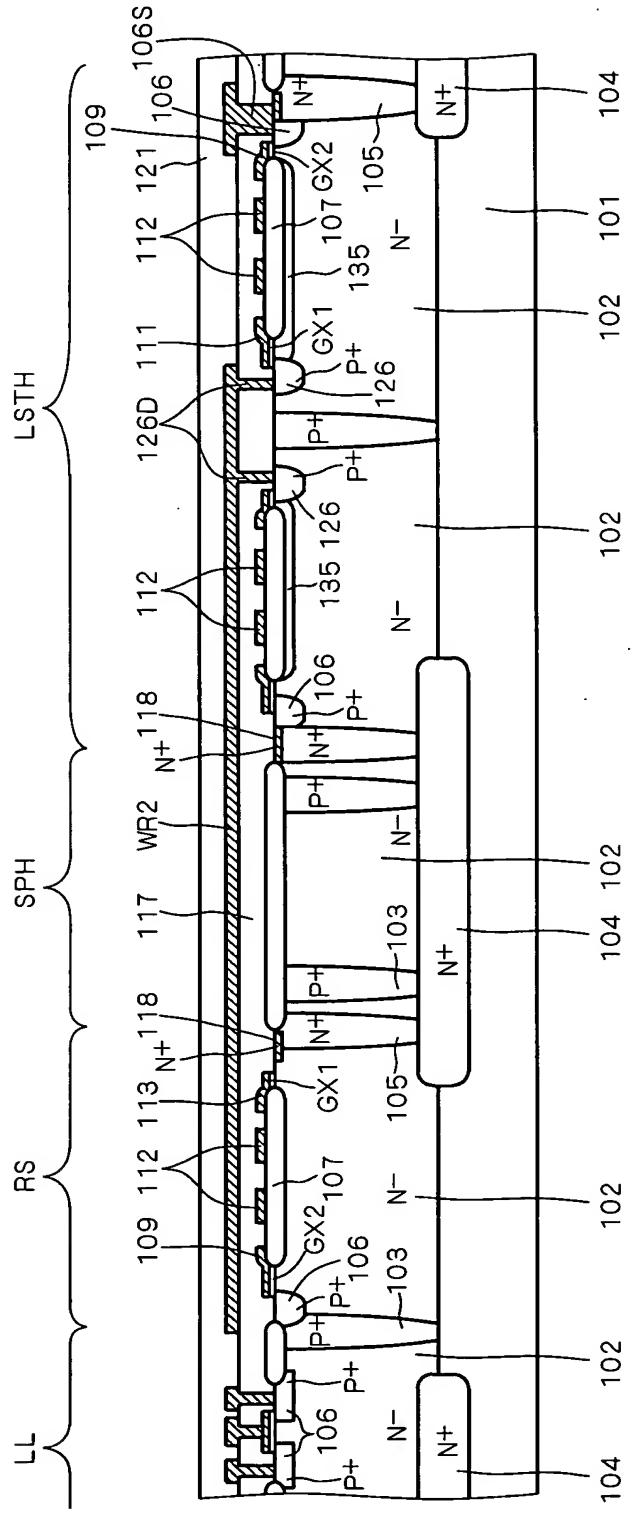


FIG. 27


LSTH
SPH
RS
LL
106S
106
109
121
112
111
126D
118
117
113
107
GX2
GX1
105
135
126
103
WR2
N+
P+
N−
104
101
102

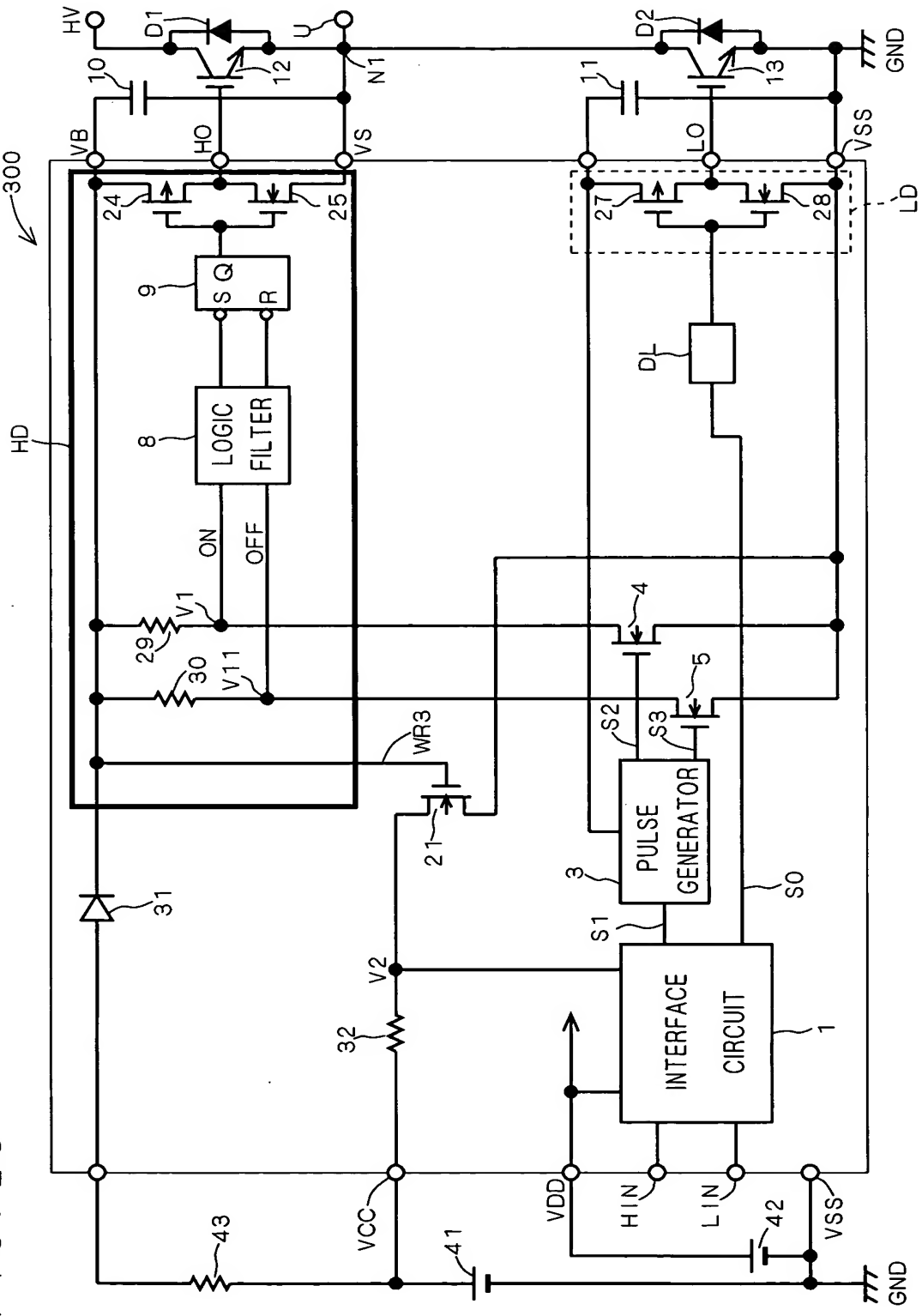

HV
D1
U
D2
GND
10
12
N1
11
13
VB
HO
VS
LO
VSS
300
24
25
27
28
LD
9
S
Q
R
DL
HD
8
LOGIC
FILTER
ON
OFF
V1
29
30
V11
4
5
S2
S3
WR3
21
PULSE
GENERATOR
3
S0
S1
31
V2
32
INTERFACE
CIRCUIT
1
VDD
HIN
LIN
VSS
42
43
VCC
41
GND

FIG. 28

FIG. 29

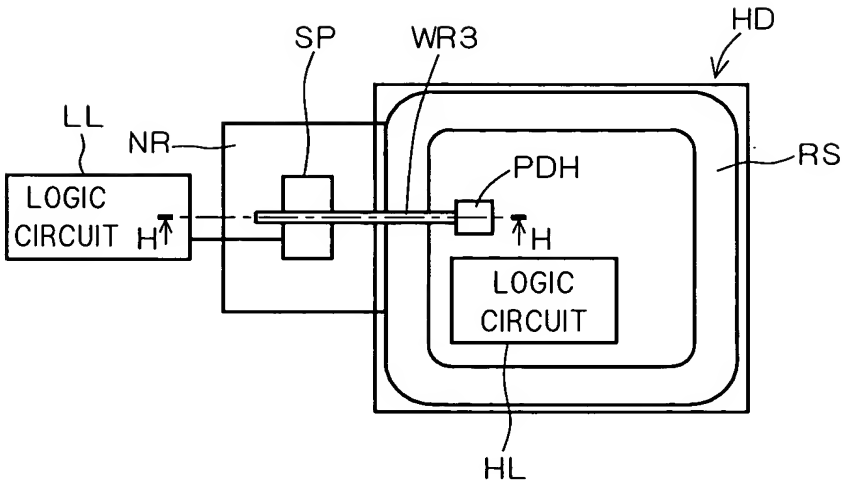
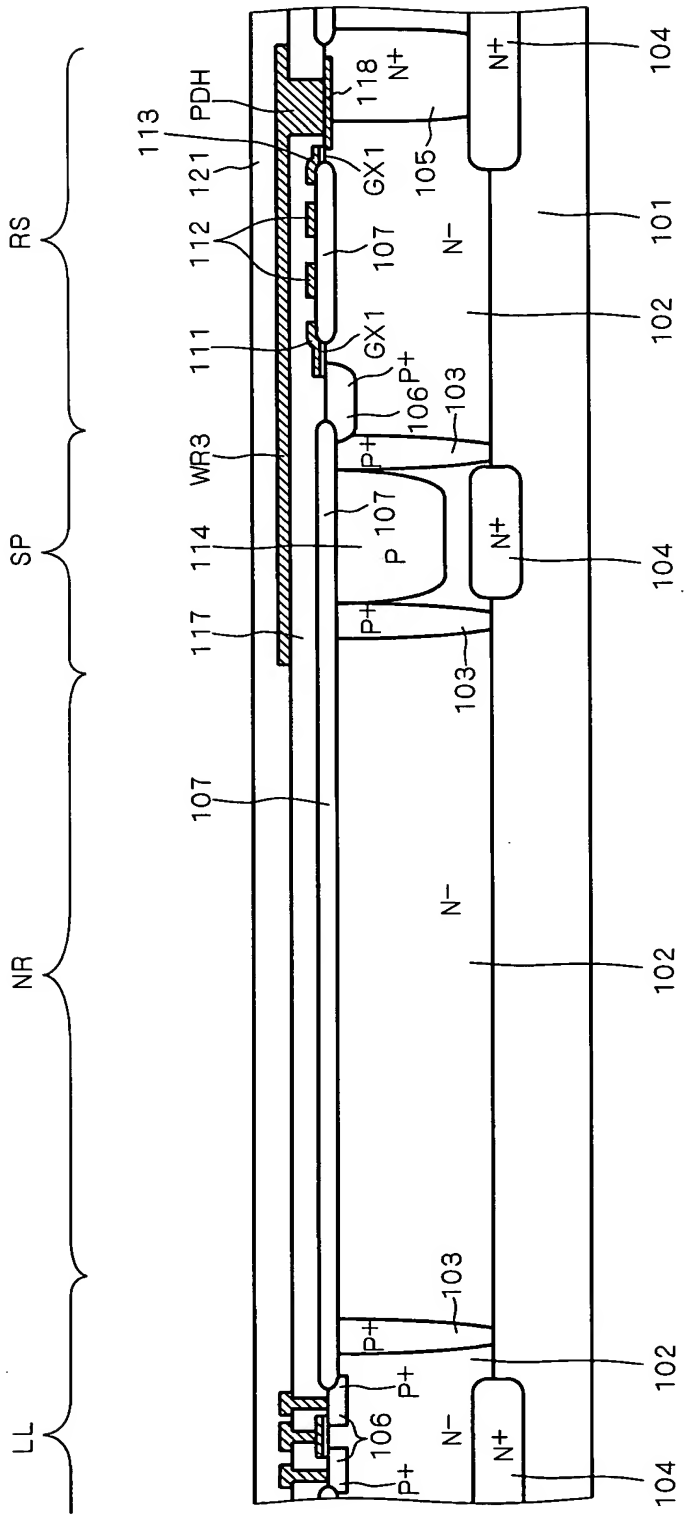


FIG. 30


RS
SP
NR
LL
113
PDH
121
112
111
WR3
114
117
107
118
N+
GX1
105
107
N−
101
102
GX1
106
P+
103
P+
P 107
N+
104
P+
103
N−
102
103
P+
P+
106
P+
N−
N+
104

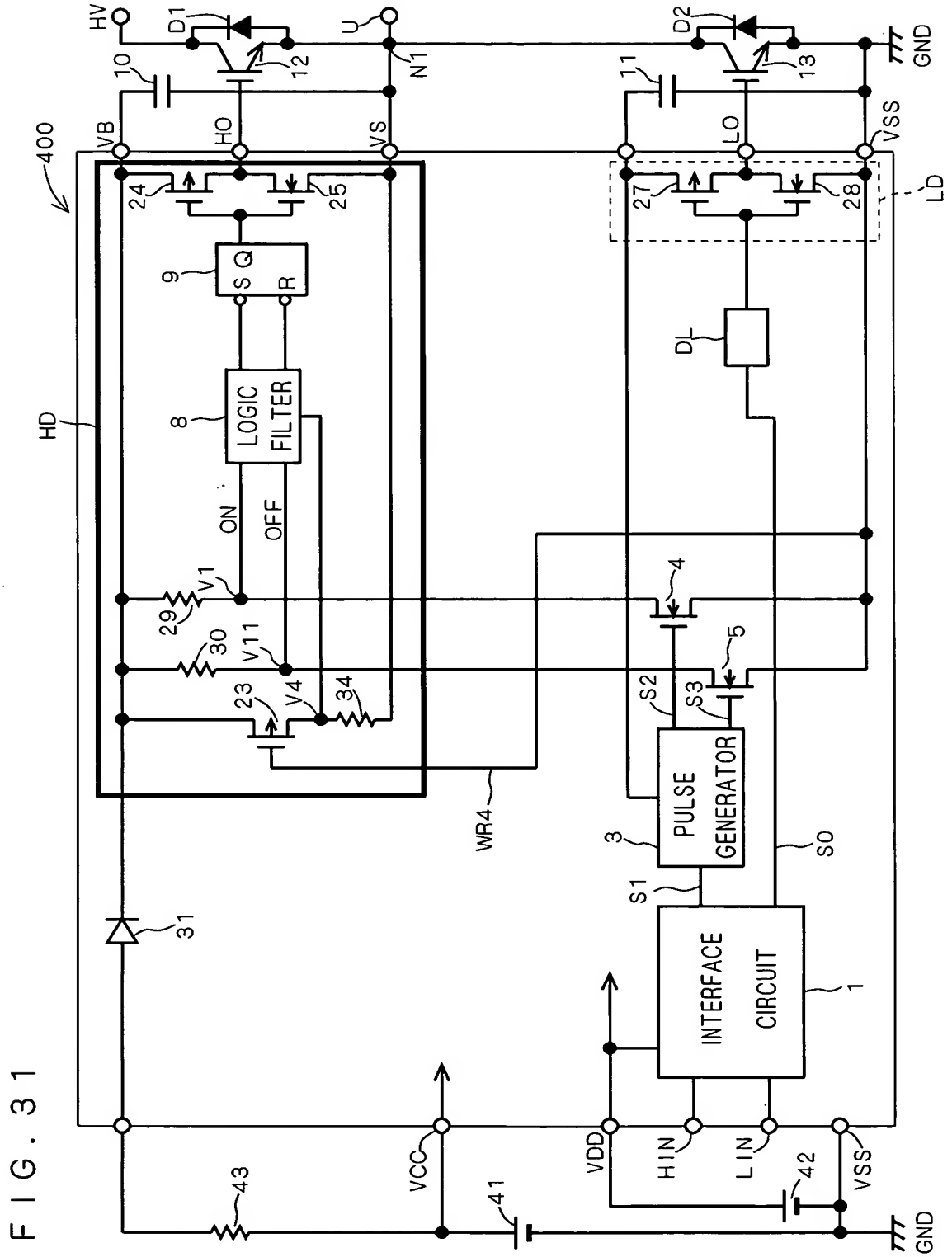

HV
D1
U
D2
GND
10
12
N1
11
13
VB
HO
VS
LO
VSS
400
LD
24
25
27
28
9
S Q
R
DL
HD
8
LOGIC FILTER
ON
OFF
V1
29
30
V11
23
V4
34
4
5
S2
S3
PULSE GENERATOR
3
WR4
S0
S1
31
INTERFACE CIRCUIT
1
VDD
HIN
LIN
VSS
42
VCC
41
43
GND

FIG. 31

FIG. 32

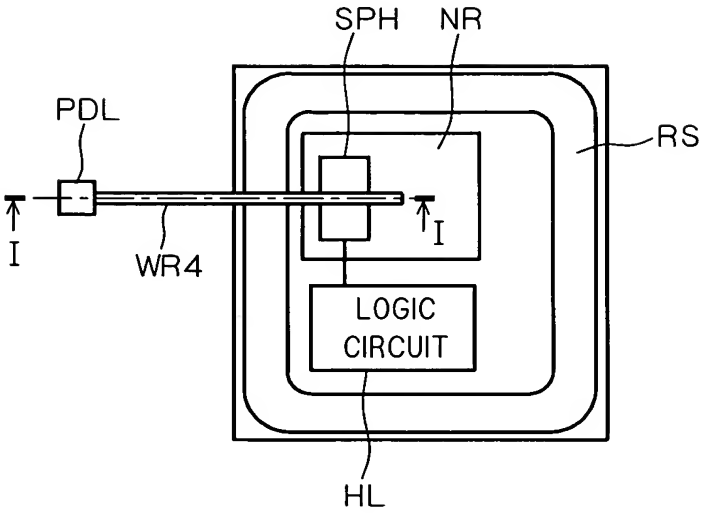
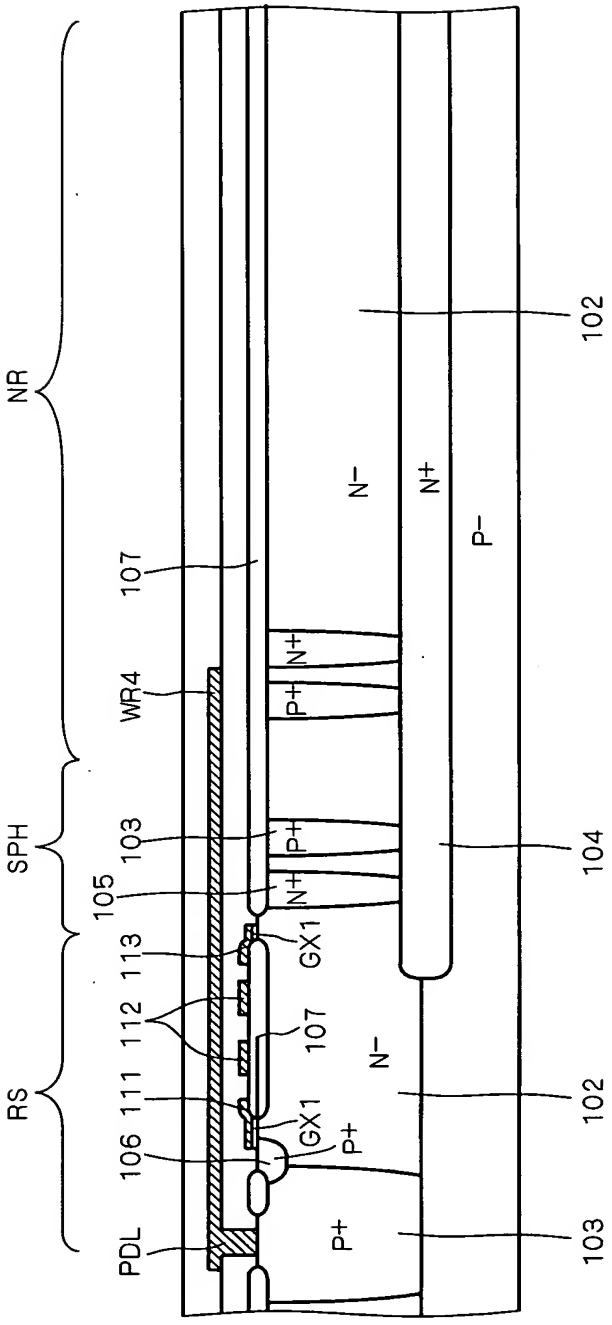


FIG. 33


NR
SPH
RS
PDL
107
WR4
103
105
113
112
111
106
N+
P+
N+
P+
GX1
107
GX1
P+
N−
N+
P−
N−
P+
102
104
102
103